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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,580	04/08/2004	Stephen L. Morein	00100.02.0003	8567

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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,580	MOREIN ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated June 13, 2006 in response to PTO Office Action dated December 28, 2005. The deletion of claim(s) 1-11 and the addition of claim(s) 12-22 have been noted and entered in the record, and applicant's remarks have been carefully considered resulting in the action as set forth herein below.

Applicant's arguments filed June 13, 2006 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,889,291 B1 to Palanca et al.

a. Regarding claim 12, Palanca et al. **discloses** a level one cache (L1 cache 120, Fig. 1), a level two cache (L2 cache 130, Fig. 1), coupled to level one cache (L1 cache 120)(...L2 cache 130 acts as an intermediary between main memory 160 and L1 cache 120...col. 4, lines 36-41). Palanca et al. discloses level two cache (L2 cache 130) supporting level one cache (L1 cache 120)(...In one embodiment L2 cache 130 is considerably larger than L1 cache 120, and may be 512 kilobytes. L2 cache 130 supports L1 cache 120...col. 4, lines 17-21). The specification of the instant application defines L1 cache and L2 cache functionality such that data requested can be quickly obtained from L2 cache as a result of it being stored therein (...the present invention is directed to a memory architecture

comprising, a main memory; a level on (L1) cache, coupled to the main memory, for maintaining information; and a level two (L2) cache, coupled between the main memory and the level one (L1) cache. The L2 cache captures overlapping requests to the main memory and the corresponding data provided thereby for subsequent use; thereby, reducing the external memory bandwidth requirements of a corresponding graphics processor. By storing the data associated with overlapping memory requests, a subsequent request for previously requested information can be quickly obtained from the L2 cache, instead of having to use valuable processing time obtaining the same information from the main memory...sheet 3, lines 7-16). Thus, "overlapping fetched texel information" is data that was fetched from main memory 160 and stored in L2 cache 130, and is thus readily available for a subsequent request in L2 cache for consumption (...L2 cache 130 acts as an intermediary between main memory 160 and L1 cache 120, and has greater storage ability than L1 cache 120, but may have a slower access speed. Loading of data from main memory 160 into multi-processor device 110 goes through L2 cache 130. L2 cache 130 can be subdivided so that processors within device 110 may share L2 cache 130 resources, thus, allowing higher system performance for the same available memory bandwidth. For example, graphics processor 113 and CPU 111 may access L2 cache 130 simultaneously without degrading the bandwidth or latency of CPU 111...col. 4, lines 36-49). Although Palanca et al. **does not explicitly disclose** level one and level two caches specifically for texel information, such use of caches for graphics data such as texel information is well known in the graphics processing art. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to make use of L1 and L2 cache of Palanca for texel information storage **because** it allows for faster accessing of graphics data and system performance improves.

b. Regarding claim 13, Palanca et al. **discloses** a cache having many blocks which individually store the various instructions and data values (...A cache has many "blocks" which individually store the various instructions and data values. The blocks in any cache are divided into groups of blocks called "sets"...col. 1, lines 19-37). Palance et al. **further discloses** multi-level caches which are interconnected (...Although Fig. 1 depicts only a two-level cache hierarchy, multi-level cache hierarchies can be provided where there are many levels of interconnected caches...col. 4, lines 13-23). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to have blocks in cache receive subsequent texel fetch instruction which is a well known two-level cache function.

c. Regarding claim 14, Palanca et al. **discloses** a main memory (main memory 160) operatively coupled to the level two cache (...L2 cache 130 acts as an intermediary between main memory 160 and L1 cache 120...Loading of data from main memory 160 into multiprocessor device 110 goes through L2 cache 130...col. 4, lines 36-40). Palanca et al. **further discloses** wherein when the level one cache and the level two cache do not comprise texel information requested by a subsequent memory fetch instruction or in other words there is a cache miss from level one and level two caches, the main memory (main memory 160) is operative to transmit the data request to level two cache for storage (...when data sought by CPU 111 or graphics processor 113 is not already in the L2 cache 130 or L1 cache...needs to be extracted from main memory 160...col. 8, lines 39-47).

d. Regarding claim 15, Palanca et al. **discloses** L2 cache 120 supporting L1 cache 120 as a two-level cache hierarchy (...L2 cache 130 supports L1 cache 120...col. 4, lines 19-20;...L2 cache 130 acts as an intermediary between main memory 160 and L1 cache 120...col. 4, lines 36-37). Although, Palanca et al. **does not explicitly disclose** level

two cache transmitting cache information as a result of fetch instruction to the level one cache for storage, it would have been obvious to a person of ordinary skill in the art at the time invention was made to consider this operation as part of multi-level cache hierarchy functionality which is well known in multi-level cache operations.

e. Regarding claims 16 and 17, Palanca et al. **discloses** a graphics controller (graphics processor 113, Fig. 1) operative to send requests to the main memory (...when data sought by CPU 111 or graphics processor 113 is not already in the L2 cache 130 or L1 cache...needs to be extracted from main memory 160...col. 8, lines 39-47); and the rest of the claim limitations is similar to claim 12 above and is rejected under the same rationale.

f. Regarding claim 19, it is similar in scope to claim 15 above and is rejected under the same rationale.

g. Regarding claim 20, it is similar in scope to claim 13 above and is rejected under the same rationale.

h. Regarding claim 21, it is similar in scope to claim 14 above and is rejected under the same rationale.

i. Regarding claim 22, it is similar in scope to claim 15 above and is rejected under the same rationale.

4. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,889,291 B1 to Palanca et al. as applied to claim 12 above, and further in view of US 6,195,106 B1 to Deering et al.

a. Regarding claim 18, Palanca et al. **is silent about** graphics controller sending requests to plurality of cache blocks, and the level two cache storing those requests being sent to the plurality of cache blocks. Deering et al. **discloses** a graphics controller (rendering controller 70, Fig. 1) sending writes to each L1 cache block which are

subsequently transferred to the memory (DRAM banks A-D) through a level two (L2) pixel cache, thereby storage of such requests at level two (L2) pixel cache is disclosed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the Palanca et al. with the feature "writes to cache blocks which are transferred to the memory" as taught by Deering et al. **because** this avoids having to access the main memory unless absolutely required (if level two cache does not have the requested data) and thus miss costs are minimized resulting in improved graphics operations (col. 10, lines 34-60).

Conclusion

5. Applicant's arguments presented are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792.** The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner , Art Unit 2628

dks
October 18, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER